REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-27 are pending in the present application. Claims 1, 6, 11, 16, and 20 are amended, without introduction of new matter, by the present amendment.

In the outstanding Office Action, Claims 1-4, 6-9, 11-14, and 16-23 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,333,750 to Odryna et al. (hereinafter "Odryna"); Claims 5, 10, and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Odryna in view of U.S. Patent No. 6,157,415 to Glen (hereinafter "Glen"); and Claims 24-27 were rejected under 35 U.S.C. § 103(a) as unpatentable over Odryna.

Applicants and Applicants' representatives thank Examiners Wang and Brier for the courtesy of the interview conducted June 24, 2004. During the interview, the features of the independent claims were discussed in view of the Odryna reference. No agreement was reached.

Addressing now, the rejection of Claims 1-27 under 35 U.S.C. § 102(e) and § 103(a) as anticipated by or unpatentable over Odryna, summarized above, those rejections are respectfully traversed.

Amended Claim is directed to an overlay image processing device for generating an overlay image signal composed of an n number of selected image signals, n being an integer greater than 2. The overly image processing device includes:

> a plurality of digital decoders configured to digitally decode a plurality of image signals;
>
> an image selector configured to directly receive outputs from each of the plurality of digital decoders and configured to select from among the plurality of digitally decoded image signals one (1) reference image signal and (n-1) number of superimposing image signals;
>
> a plurality of resolution converters configured to directly receive the selected image signals output from the image selector, ***such that each***

> ***resolution converter can input any of the respective outputs***, to convert resolutions of the n number of selected image signals into respective desired resolutions, and to output the converted image signals to an image synthesizer,
>
> wherein the image synthesizer is configured to superimpose the (n-1) number of converted superimposing image signals on the converted one (1) reference signal, and
>
> ***the image selector is configured to connect each of the digital decoders to any of the resolution converters.***

As emphasized, (1) each of the resolution converters can input any of the respective outputs of the digital decoders, and (2) the image selector is configured to connect each of the digital decoders to any of the resolution converters. Amended independent Claims 6, 11, 16, and 20 similarly recite features (1) and (2). The remaining pending claims depend directly or indirectly from Claims 1, 6, 11, 16, and 20.

In a non-limiting example, Figure 2 of the present application illustrates an embodiment of the claimed invention. As shown, an image selector 116 permits each of the image signals VPC(D), VS1(D), and VS2(D), which are output by their respective digital decoders 110, 112, and 114, to be relayed to any of the resolution converters 118 and 120. Thus, the selector 116 can select two image signals from among any of the three original digitized image signals VPC(D), VS1(D), and VS2(D), according to the user's instructions. Further, one of the two selected image signals is designated as a reference original image signal SD10 input to resolution converter 118 and the other as a superimposing original image signal SD20 input to resolution converter 120.[1] In this respect, the image selector provides a singular, centrally arranged component that connects each of the digital decoders to each of the resolution converters.

The outstanding Office Action cites Odryna as teaching the claimed image selector. During the above-noted interview, Examiner Wang stated that the control block 111 of Odryna can be connected (via the serial control bus 113) to a plurality of control arrays 188,

[1] Specification, page 6, line 18-24.

memories 0, 1, and SWITCHes of respective BIVIDEO cards 180; and stated that these assorted components collectively form "an image selector" that receives image signals from the respective decoders 182 of those input cards 180. Examiner Wang further stated that the signals could be directly output from the SWITCHes (which comprise part of the proposed "image selector") to the respective scalers 184 of the input cards 180 (because the scaler 180 is alternatively taught as arranged after the memory of those cards 180).

Respectfully, Applicants first note the proposed assortment of Odryna's components does not teach a single "image selector". Rather, the proposed assortment of components is part of Odryna's distributed system. This distinction is further emphasized by features (1) and (2) of the claimed invention, as noted above, because only a central system of components for selecting (as opposed to a distributed system of components for selecting) can receive signals from each of the digital decoders and relay those respective outputs to any of the resolution converters (i.e., can connect each of the decoders to any of the resolution converters).

The Office Action also cites Odryna as teaching the claimed digital decoders and resolution converters. More particularly, the Office Action cites the broadcast video decoder 182 and scaler 184 of Odryna's video cards (see Figure 21) as teaching the claimed plurality of digital decoders and resolution converters, respectively; and the Action asserts that the arrangement of a plurality of video cards, such as input cards A, B, C (see Figure 17) each having one decoder 182 and one scaler 184 (see Figure 21), results in a system teaching the claimed plurality of digital decoders and resolution converters. However, such an arrangement of video cards leaves each decoder 182 connected to one, and only one, respective scaler 184. Accordingly, this one-to-one relationship between each decoder 182 and respective scaler 184 precludes Odryna from attaining the configuration recited by features (1) and (2) of the claimed invention.

Accordingly, for the reasons stated above, Applicants respectfully request that the rejection of Claims 1-27, under § 102(e) and § 103(a) as anticipated by or unpatentable over Odryna, be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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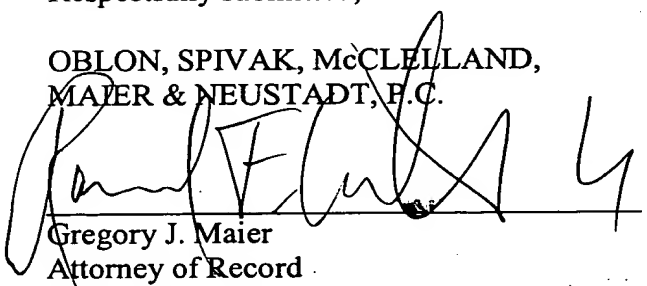

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